

# Silicon Carbide Substrates and Epitaxy

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## Product Specifications

4H Silicon Carbide Substrates  
N-type, P-type, and Semi-Insulating

N-type and P-type Silicon Carbide Epitaxy



## Physical Properties

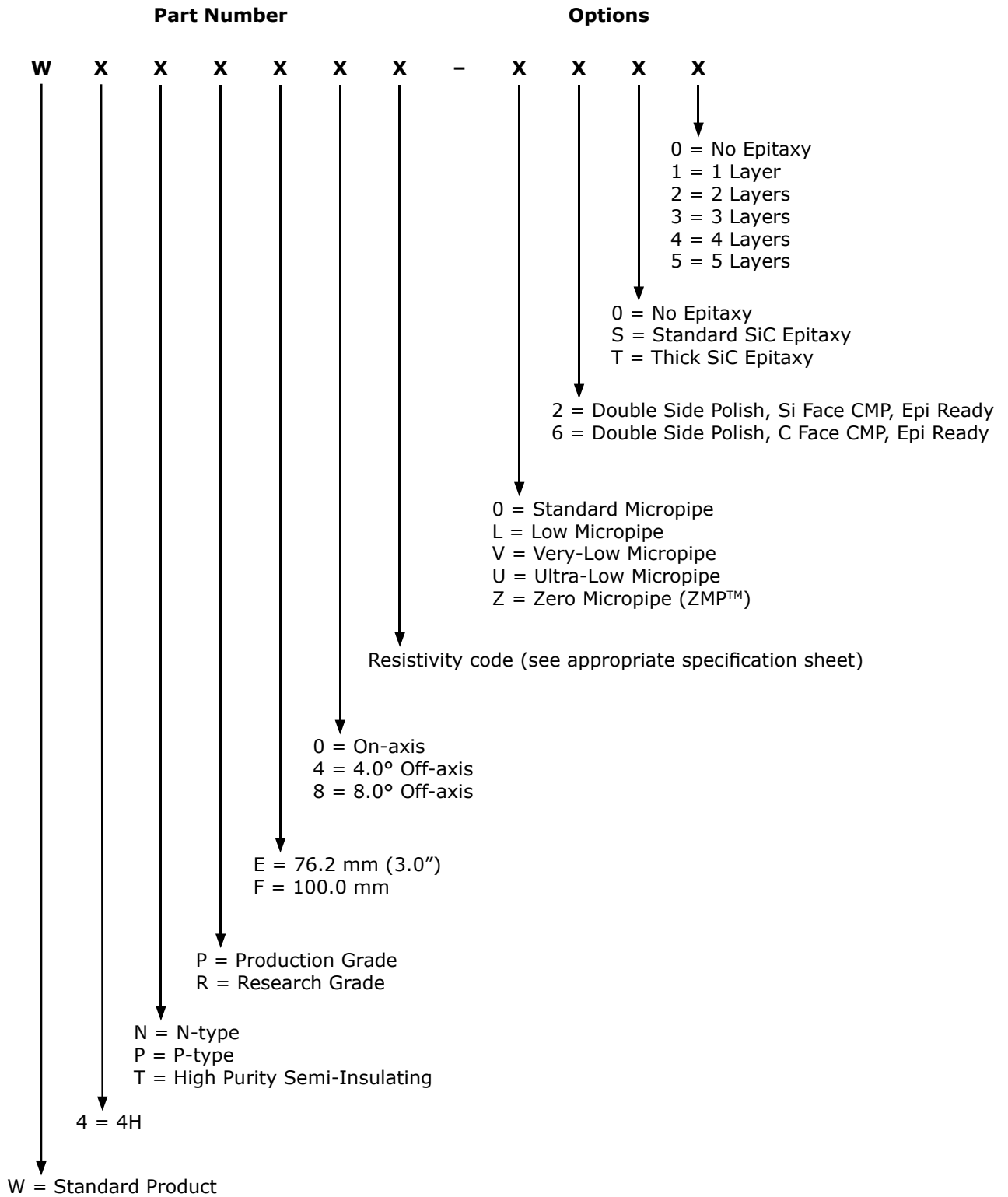
Polytype	Single Crystal 4H
Crystal Structure	Hexagonal
Bandgap	3.26 eV
Thermal Conductivity (n-type; 0.020 ohm-cm)	a~4.2 W/cm • K @ 298 K c~3.7 W/cm • K @ 298 K
Thermal Conductivity (HPSI)	a~4.9 W/cm • K @ 298 K c~3.9 W/cm • K @ 298 K
Lattice Parameters	a=3.073 Å c=10.053 Å
Mohs Hardness	~9

## Applications

- High-Power Devices
- High-Frequency Power Devices
- III-V Nitride Deposition
- High-Temperature Devices
- Optoelectronic Devices



## Product Descriptions





## Product Descriptions - 76.2 mm Silicon Carbide

### 76.2 mm Diameter 4H Silicon Carbide

Part Number	Type	Orientation	Micropipe Density	Resistivity Ohm-cm Range	Bin
<b>N-TYPE LOW MICROPIPE DENSITY</b>					
W4NxE4C-L200	N	4° Off	≤ 15 micropipes/cm <sup>2</sup>	0.015-0.028	C
W4NxE8C-L200	N	8° Off	≤ 15 micropipes/cm <sup>2</sup>	0.015-0.028	C
<b>N-TYPE VERY-LOW MICROPIPE DENSITY</b>					
W4NxE4C-V200	N	4° Off	≤ 5 micropipes/cm <sup>2</sup>	0.015-0.028	C
W4NxE8C-V200	N	8° Off	≤ 5 micropipes/cm <sup>2</sup>	0.015-0.028	C
<b>N-TYPE ULTRA-LOW MICROPIPE DENSITY</b>					
W4NxE4C-U200	N	4° Off	≤ 1 micropipes/cm <sup>2</sup>	0.015-0.028	C
W4NxE8C-U200	N	8° Off	≤ 1 micropipes/cm <sup>2</sup>	0.015-0.028	C
<b>N-TYPE ZERO MICROPIPE DENSITY (ZMP™)</b>					
W4NxE4C-Z200	N	4° Off	0 micropipes/cm <sup>2</sup>	0.015-0.028	C
<b>N-TYPE LCW</b>					
W4NRE0X-0200	N	On-axis	N/A	0.013-2.000	N/A
<b>P-TYPE</b>					
W4PRE8F-0200	P	8° Off	N/A	≤2.5	F
<b>HIGH PURITY SEMI-INSULATING</b>					
W4TRE0R-0200	HPSI	On-axis	N/A	≥ 1E5	R
W4TRE8R-0200	HPSI	8° Off	N/A	≥ 1E5	R



## Product Descriptions - 100.0 mm Silicon Carbide

### 100.0 mm Diameter 4H Silicon Carbide

Part Number	Type	Orientation	Micropipe Density	Resistivity Ohm-cm Range	Bin
<b>N-TYPE LOW MICROPIPE DENSITY</b>					
W4Nx4C-L200	N	4° Off	≤ 15 micropipes/cm <sup>2</sup>	0.015-0.028	C
<b>N-TYPE VERY-LOW MICROPIPE DENSITY</b>					
W4Nx4C-V200	N	4° Off	≤ 5 micropipes/cm <sup>2</sup>	0.015-0.028	C
<b>N-TYPE ULTRA-LOW MICROPIPE DENSITY</b>					
W4Nx4C-U200	N	4° Off	≤ 1 micropipes/cm <sup>2</sup>	0.015-0.028	C
<b>N-TYPE ZERO MICROPIPE DENSITY (ZMP™)</b>					
W4Nx4C-Z200	N	4° Off	0 micropipes/cm <sup>2</sup>	0.015-0.028	C
<b>N-TYPE LCW</b>					
W4NRF0X-0200	N	On-axis	N/A	0.013-2.000	N/A
<b>HIGH PURITY SEMI-INSULATING</b>					
W4TRF0R-0200	HPSI	On-axis	N/A	≥ 1E5	R

## Standard Specifications

### Definition of Dimensional Properties, Terminology and Methods

#### Diameter

The linear dimension across the surface of a wafer. Measurement is performed manually with ANSI certified digital calipers on each individual wafer (See Figure 1).

#### Thickness, Center Point

Measured with ANSI certified non-contact tools at the center of each individual wafer.

#### Flat Length

Linear dimension of the flat measured with ANSI certified digital calipers on a sample of one wafer per ingot (See Figure 1).

#### Surface Orientation

Denotes the orientation of the surface of a wafer with respect to a crystallographic plane within the lattice structure. In wafers cut intentionally "off orientation", the direction of cut is parallel to the primary flat, away from the secondary flat. Measured with x-ray goniometer on a sample of one wafer per ingot in the center of the wafer.

#### Orthogonal Misorientation

In wafers cut intentionally "off orientation", the angle between the projection of the normal vector to the wafers surface onto a  $\{0001\}$  plane and the projection on that plane of the nearest  $\langle 11\bar{2}0 \rangle$  direction.

#### Primary Flat

The primary flat is the  $\{10\bar{1}0\}$  plane with the flat face parallel to the  $\langle 11\bar{2}0 \rangle$  direction.

#### Primary Flat Orientation

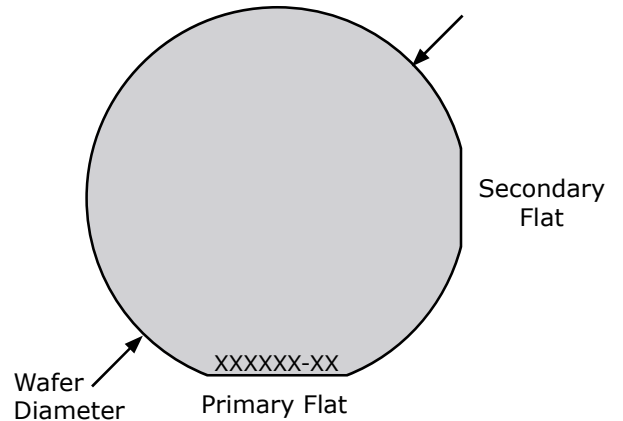
The flat of the longest length on the wafer, oriented such that the chord is parallel with a specified low index crystal plane. Measured on one wafer per ingot using Laue back-reflection technique with manual angle measurement.

#### Secondary Flat Orientation

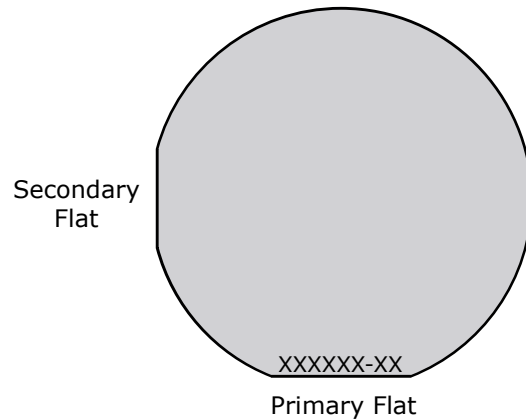
A flat of shorter length than the primary orientation flat, whose position with respect to the primary orientation flat identifies the face of the wafer.

#### Marking

For silicon face polished material, the carbon face of each individual wafer is laser marked with OCR compatible font, similar to definitions and characteristics in SEMI M12 (See Figure 1). For carbon face polished material, the silicon face of each individual wafer is laser marked (See Figure 2).



**Figure 1. Diameter, Primary and Secondary Flat Locations, and Marking Orientation, Carbon Face Up for Silicon Face Polished Wafers**



**Figure 2. Primary and Secondary Flat Locations, and Marking Orientation, Silicon Face Up for Carbon Face Polished Wafers**



## Standard Specifications

### 76.2 mm Diameter Substrate Specifications

SUBSTRATE PROPERTY	CREE STANDARD
<b>Diameter</b>	3.000" ± 0.015" 76.2 mm ± 0.38 mm
<b>Thickness N-type on-axis</b>	0.0145" ± 0.0025" 368.0 μm ± 64.0 μm
<b>Thickness N-type off-axis; Semi-Insulating</b>	0.0138" ± 0.001" 350.0 μm ± 25.0 μm
<b>Dopant</b>	n-type: Nitrogen
<b>Primary Flat Length</b>	0.875" ± 0.125" 22.22 mm ± 3.17 mm
<b>Secondary Flat Length</b>	0.440" ± 0.060" 11.18 mm ± 1.52 mm
<b>Surface Orientation On-axis</b>	{0001} ± 0.25°
<b>Surface Orientation Off-axis</b>	4.0° toward $\langle 11\bar{2}0 \rangle$ ± 0.5° 8.0° toward $\langle 11\bar{2}0 \rangle$ ± 0.5°
<b>Surface Finish</b>	Both sides polished
<b>Orthogonal Misorientation</b>	± 5.0°
<b>Primary Flat Orientation</b>	$\langle 11\bar{2}0 \rangle$ ± 5.0°
<b>Secondary Flat Orientation</b>	90.0° CW from Primary ± 5.0°, Silicon Face Up
<b>TTV</b>	≤ 15 microns, Full Substrate
<b>Warp</b>	≤ 35 microns, Full Substrate
<b>LTV (Average, 1cm<sup>2</sup> Site)</b>	≤ 4 microns, Full Substrate
<b>Packaging</b>	Multi-Wafer Box unless otherwise specified



## Standard Specifications

### 100.0 mm Diameter Substrate Specifications

SUBSTRATE PROPERTY	CREE STANDARD
Diameter	100.0 mm +0.0/-0.5 mm
Thickness N-type on-axis	500.0 $\mu\text{m}$ $\pm$ 50.0 $\mu\text{m}$
Thickness N-type off-axis	350.0 $\mu\text{m}$ $\pm$ 25.0 $\mu\text{m}$
Thickness Semi-Insulating	500.0 $\mu\text{m}$ $\pm$ 25.0 $\mu\text{m}$
Dopant	n-type: Nitrogen
Primary Flat Length	32.5 mm $\pm$ 2.0 mm
Secondary Flat Length	18.0 mm $\pm$ 2.0 mm
Surface Orientation On-axis	{0001} $\pm$ 0.25°
Surface Orientation Off-axis	4.0° toward $\langle 11\bar{2}0 \rangle$ $\pm$ 0.5°
Surface Finish	Both sides polished
Orthogonal Misorientation	$\pm$ 5.0°
Primary Flat Orientation	$\langle 11\bar{2}0 \rangle$ $\pm$ 5.0°
Secondary Flat Orientation	90.0° CW from Primary $\pm$ 5.0°, Silicon Face Up
TTV	$\leq$ 15 microns, Full Substrate
Warp	$\leq$ 45 microns, Full Substrate
LTV (Average, 1cm <sup>2</sup> Site)	$\leq$ 4 microns, Full Substrate
Packaging	Multi-Wafer Box unless otherwise specified





## Standard Specifications

### Standard Specifications for Polished Silicon Carbide Substrates – Surface Finish

Characteristics	Production Grade	Research Grade
<b>Edge Chips/Indents by diffuse lighting†</b>	None Permitted	2 ≤ 1.0 mm width & depth
<b>Orange Peel/Pits by diffuse lighting*◇</b>	≤ 10% area	≤ 30% area
<b>Polytype Areas by diffuse lighting*</b>	≤ 5% area	≤ 20% area
<b>Striations by diffuse lighting</b>	3 allowed ≤ 3 mm each	20 allowed ≤ 7 mm each
<b>Area Contamination (stains) by high intensity light</b>	None permitted	None permitted
<b>Cracks by high intensity light</b>	None permitted	None permitted
<b>Hex Plates by high intensity light*</b>	Cumulative area < 10%	Cumulative area < 30%
<b>Scratches by high intensity light*</b>	5 scratches to 1x wafer diameter cumulative length	8 scratches to 1.5x wafer diameter cumulative length
<b>Masking Defects (Mounds)*</b> Quantitative by 200x Microscopic Inspection	10 defects in 3 or less of the 9 fields inspected in a cross pattern	10 defects in 5 or less of the 9 fields inspected in a cross pattern
<b>Contamination</b> Quantitative by 200x Microscopic Inspection	None in inspected fields	None in inspected fields
<b>Cumulative Area Defects*</b>	≤ 10% area	≤ 30% area

**Notes:**

\* Defect limits apply to entire wafer surface except for edge exclusion area, which is 2 mm for 76.2 mm substrates and 3 mm for 100.0 mm substrates.

◇ Pits must be < 2 mm in distance from one another to be considered a reject cause.

+ Edge chips must be > 0.5 mm on R grade material to be considered a reject cause.



## Standard Specifications for Polished Silicon Carbide Substrates – Surface Finish

### Definition of Terminology and Methods

#### (Area) Contamination

Any foreign matter on the surface in localized areas which is revealed under high intensity (or diffuse) illumination as discolored, mottled, or cloudy appearance resulting from smudges, stains or water spots.

#### Cracks

A fracture or cleavage of the wafer that extends from the frontside surface of the wafer to the back-side surface of the wafer. Cracks must exceed 0.010" in length under high intensity illumination in order to discriminate fracture lines from allowable crystalline striations. Fracture lines typically exhibit sharp, thin lines of propagation, which discriminate them from material striations.

#### Edge Chips

Any edge anomalies (including wafer saw exit marks) in excess of 1.0 mm in either radial depth or width. As viewed under diffuse illumination, edge chips are determined as unintentionally missing material from the edge of the wafer.

#### Edge Exclusion

The outer annulus of the wafer is designated as wafer handling area and is excluded from surface finish criteria (such as scratches, pits, haze, contamination, craters, dimples, grooves, mounds, orange peel and saw marks). This annulus is 2 mm for 76.2 mm substrates, and 3 mm for 100.0 mm substrates.

#### Hex Plate

Hexagonal shaped platelets on the surface of the wafer which appear silver in color to the unaided eye, under diffuse illumination.

#### Masking Defects (also referred to as "Mound")

A distinct raised area above the wafer frontside surface as viewed with diffuse illumination.

#### Orange peel

Visually detectable surface roughening when viewed under diffuse illumination.

#### Pits

Individual distinguishable surface anomalies, which appears as a depression in the wafer surface with a length-to-width ratio less than 5 to 1, and visible under high intensity illumination.

#### Foreign Polytypes (also referred to as "Inclusions" or "Crystallites")

Regions of the wafer crystallography which are polycrystalline or of a different polytype material than the remainder of the wafer, such as 6H mixed in with a 4H type substrate. Foreign polytype regions frequently exhibit color changes or distinct boundary lines, and are judged in terms of area percent under diffuse illumination.

#### Scratches

A scratch is defined as a singular cut or groove into the frontside wafer surface with a length-to-width ratio of greater than 5 to 1, and visible under high intensity illumination.

#### Striations

Striations in silicon carbide are defined as linear crystallographic defects extending down from the surface of the wafer which may or may not pass through the entire thickness of the wafer, and generally follow crystallographic planes over its length.

#### Total Usable Area

A cumulative subtraction of all noted defect areas from the frontside wafer quality area within the edge exclusion zone. The remaining percent value indicates the proportion of the frontside surface to be free of all noted defects (does not include edge exclusion).



## Specifications for Silicon Carbide Epitaxy

### Standard Specifications for Silicon Carbide Epitaxial Wafer – 76.2 mm and 100.0 mm Substrates

<b>Substrate Orientation:</b> Epitaxy is only available for off-axis substrates		
<b>Conductivity</b>	n-type	p-type
<b>Dopant</b>	Nitrogen	Aluminum
<b>Net Doping Density</b>	$N_D - N_A$	$N_A - N_D$
Silicon Face	9E14 – 1E19/cm <sup>3</sup>	9E14 – 1E19/cm <sup>3</sup>
Carbon Face	1E16 – 1E19/cm <sup>3</sup>	Not available
Tolerance	± 25%	± 50%
<b>Thickness Range – Silicon Face</b>		
0.2-50.0 microns	± 10% of selected thickness	± 10% of selected thickness
<b>Thickness Range – Carbon Face</b>		
0.2-1.0 microns	± 25% of selected thickness	Not available
1.0-10.0 microns	± 15% of selected thickness	Not Available

**Notes:**

- 2 mm edge exclusion for 76.2 mm, 3 mm edge exclusion for 100.0 mm
- N-type epi layers <20 microns are preceded by n-type , 1E18, 0.5 micron buffer layer
- N-type epi layers ≥20 microns are preceded by n-type , 1E18, 1.0 micron buffer layer
- No buffer layer for p-type epitaxial layers
- Not all doping densities are available in all thicknesses
- Contact Cree Sales for specifications on multi-layer or unique epitaxy requests



## Specifications for Silicon Carbide Epitaxy

### Standard Specifications for Silicon Carbide Epitaxial Wafer – 76.2 mm and 100.0 mm Substrates

Characteristics	Maximum Acceptability Limits		Test Methods	Defect Definitions (see pg. 14)	Methodology (see pg. 15)	
Large Point Defects	76.2 mm	60	Diffuse Illumination	D1	M1, M2	
	100.0 mm	90				
Scratches	10 lines < 2x wafer diameter			D2		
Dimpling	< 5% affected			D3		
Step Bunching	4.0° off-axis	N/A		D4		
	8.0° off-axis	< 10% affected				
Backside Cleanliness	95% clean			D5		
Edge Chips	2 with radius 1.5 mm			D6		
ID Correct/Legible	Yes			D7		M2
Wafer Flats	Yes					
Epi Defects	25/cm <sup>2</sup>		Microscopic	D8-D12	M3	
Net Doping	See Specification Table		Hg Probe CV	-	M4	
Thickness	See Specification Table		FTIR	-	M5	

**Notes:**

- 2 mm edge exclusion for 76.2 mm, 3 mm edge exclusion for 100.0 mm



## Specifications for Silicon Carbide Epitaxy

### Standard Specifications for Silicon Carbide Epitaxial Wafer, Definitions, Epitaxy Defect Descriptions and Methodology

#### Definitions

##### D1. Large Point Defects

Defects which exhibit a clear shape to the unassisted eye and are > 50 microns across. These features include spikes, adherent particles, chips and craters. Large point defects less than 3 mm apart count as one defect.

##### D2. Scratches

Grooves or cuts below the surface plane of the wafer having a length-to-width ratio of greater than 5 to 1. Scratches are specified by the number of discrete scratches times the total length in fractional diameter.

##### D3. Dimpling

A texture resembling the surface of a golf ball. Specified in % affected area.

##### D4. Step Bunching

Step bunching is visible as a pattern of parallel lines running perpendicular to the major flat. If present, estimate the % of specified area affected.

##### D5. Backside Cleanliness

Verified by inspecting for a uniform color to the wafer backside. Note there is a darker region near the center of some higher doped wafers. Backside cleanliness specified as percent area clean.

##### D6. Edge Chips

Areas where material has been unintentionally removed from the wafer. Do not confuse fractures in epi crown with edge chips.

##### D7. ID Correct and Major Wafer Flat

Both should be readily discernible.

#### Epitaxy Defects

The sum of discrete microscopic defects counted in specified area. These include 3C inclusions, comet tails, carrots, particles and silicon droplets.

##### D8. 3C Inclusions

Regions where step-flow was interrupted during epi layer growth. Typical regions are generally triangular although more rounded shapes are sometimes seen. Count once per occurrence. Two inclusions within 200 microns count as one.

##### D9. Comet Tails

Comet tails have a discrete head and trailing tail. These features are aligned parallel to the major flat. Usually, all comet tails tend to be of the same length. Count once per occurrence. Two comet tails within 200 microns count as one.

##### D10. Carrots

Similar to comet tails in appearance except they are more angular and lack a discrete head. If present, these features are aligned parallel to the major flat. Usually, any carrots present tend to be of the same length. Count once per occurrence. Two carrots within 200 microns count as one.

##### D11. Particles

Particles have the appearance of eyes and if present are usually concentrated at the wafer edges and not within the specified area. If present, count once per occurrence. Two particles within 200 microns count as one.

##### D12. Silicon droplets

Silicon droplets can appear as either small mounds or depressions in the wafer surface. Normally absent, but if present are largely concentrated at perimeter of wafer. If present, estimate the % of specified area affected.

## Specifications for Silicon Carbide Epitaxy

### Standard Specifications for Silicon Carbide Epitaxial Wafer, Definitions, Epitaxy Defect Descriptions and Methodology

#### Methodology

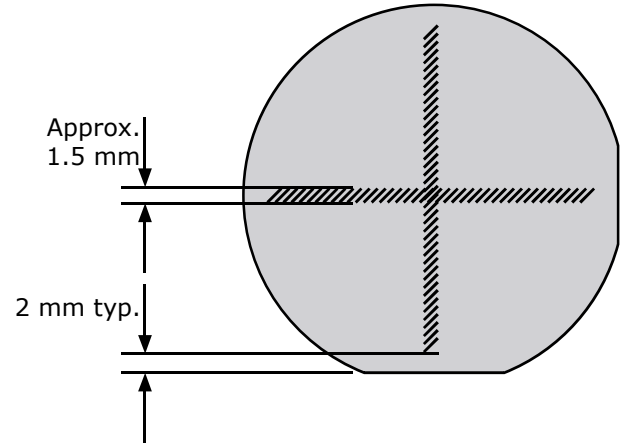
**M1.** 2 mm edge exclusion for 76.2 mm, 3 mm edge exclusion for 100.0 mm.

**M2.** Inspection performed under diffuse illumination.

**M3.** Microscopic inspection performed at 100X, on an Olympus BH2 UMA Optical Microscope, or comparable. Inspection pattern detailed in Figure 2.

**M4.** Net doping is determined as an average value of multiple points along radius opposite major flat using Hg probe CV.

**M5.** Thickness is determined as an average value across the wafer using FTIR, or mass difference.



**Figure 2. Epi Inspection Pattern**